AMENDMENTS TO THE CLAIMS:

This listing of claims replaces all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (Currently Amended) A flip-flop circuit ~~arrangement,~~ comprising

[[-]] ~~a pair of~~ input terminals ~~(CP, CN), designed for supplying~~ to provide a differential clock signal[[,]];

[[-]] ~~a pair of~~ output terminals ~~(QP, QN), designed for tapping~~ to provide a differential output signal,

[[-]] ~~four~~ differential amplifiers ~~(1, 2, 3, 4)~~, each ~~having~~ of the differential amplifiers comprising at least two transistors ~~(5, 6; 7, 8; 9, 10; 11, 12)~~, ~~whose~~ the transistors comprising collectors, each collector being part of one of plural ~~controlled sections are each positioned in a~~ series ~~circuit with~~ circuits containing a resistor ~~(R1, R2, R3, R4)~~, the series circuits being positioned between a ~~first~~ power supply potential terminal ~~(VCC)~~ and a first shared emitter node and/or a second shared emitter node ~~(E1, E2)~~, ~~whose~~ sets of the ~~control~~ collectors ~~terminals are~~ being interconnected ~~coupled to one another~~ to form a D flip-flop structure, the ~~and in which the pair of~~ output terminals ~~(QP, QN) is formed at the~~ being at an output of at least one differential amplifier; ~~(3),~~

[[-]] a first current source ~~(Q1), which connects~~ to connect the first shared emitter node ~~(E1)~~ to a reference potential terminal; ~~(VEE),~~

[[-]] a second current source ~~(Q2), which connects~~ to connect the second shared emitter node ~~(E2)~~ to the reference potential terminal; ~~(VEE),~~

[[-]] a first switch ~~(S1), whose controlled section is connected~~ between the power supply potential terminal ~~(VCC)~~ and the first shared emitter node, the first switch having a first control terminal that comprises part of the input terminals; ~~(E1),~~ and

[[-]] a second switch ~~(S2), whose controlled section is connected~~ between the supply potential terminal ~~(VCC)~~ and the second shared emitter node, the second switch having a second control terminal that comprises part of the input terminals ~~(E2),~~ ~~[[-]] the first and the second switches (S1, S2) each having a control terminal which form the pair of input terminals (CP, CN)~~.

2. (Currently Amended) The flip-flop circuit of ~~arrangement according to~~ claim 1, wherein the differential amplifiers comprise: ~~characterized in that~~

[[-]] a first differential amplifier ~~(1) is provided,~~ comprising a first pair of emitter-coupled transistors ~~(5, 6) in~~ connected to the first shared emitter node ~~(E1)~~, ~~whose~~ the first pair of emitter-coupled transistors comprising collector terminals that form at last parts of a first circuit node ~~(ON1)~~ and a second circuit node, ~~(OP1) and whose~~ the first pair of emitter-coupled transistors comprising base terminals that are cross-connected to ~~their~~ collector terminals[[,]];

[[-]] a second differential amplifier ~~(2) is provided,~~ comprising a second pair of emitter-coupled transistors ~~(7, 8) in~~ connected to the second shared emitter node ~~(E2)~~, ~~whose~~ the second pair of emitter-coupled transistors comprising collector terminals that are

connected to the first circuit node ~~(ON1)~~ and/or to the second circuit node, the second pair of emitter-coupled transistors comprising ~~(OP1) and whose~~ base terminals that form at least part of a third circuit node ~~(ON2)~~ and a fourth circuit node; ~~(OP2),~~

[[-]] a third differential amplifier ~~(3) is provided,~~ comprising a third pair of emitter-coupled transistors ~~(9, 10) in~~ connected to the second shared emitter node ~~(E2)~~, ~~whose~~ the third pair of emitter-coupled transistors comprising collector terminals that are connected to the third circuit node ~~(ON2)~~ and/or to the fourth circuit node, the third pair of emitter-coupled transistors comprising ~~(OP2) and whose~~ base terminals that are cross-connected to ~~their~~ collector terminals[[,]]; and

[[-]] a fourth differential amplifier ~~(4) is provided,~~ comprising a fourth pair of emitter-coupled transistors ~~(11, 12) in~~ connected to the first shared emitter node ~~(E1)~~, ~~whose~~ the fourth pair of emitter-coupled transistors comprising collector terminals that are connected to the third circuit node ~~(ON2)~~ and/or to the fourth circuit node, the fourth pair of emitter-coupled transistors comprising ~~(OP2) and whose~~ base terminals that are connected to the second circuit node ~~(OP1)~~ and/or to the first circuit node ~~(ON1)~~.

3. (Currently Amended) The flip-flop circuit ~~arrangement according to~~ of claim 2, ~~characterized in that~~ wherein the first, the second, the third, and the fourth circuit nodes ~~(ON1, OP1, ON2, OP2)~~ are each connected via a resistor in a series circuit ~~(R1, R2, R3, R4)~~ to the power supply potential terminal ~~(VCC)~~.

4. (Currently Amended) The flip-flop circuit ~~arrangement according to one~~ of claim 2 ~~Claims 1 through 3~~, ~~characterized in that~~ wherein the first, the second, the third, and the fourth differential amplifiers ~~(1, 2, 3, 4)~~ and the first and the second switches ~~(S1, S2)~~ are implemented ~~in~~ using bipolar circuit technology.

5. (Currently Amended) The flip-flop circuit of claim 1 ~~arrangement according to one of Claims 1 through 4~~, ~~characterized in that~~ wherein the first current source and the second current source ~~(Q1, Q2)~~ each comprise a transistor ~~in~~ implemented using metal oxide semiconductor circuit technology.

6. (Currently Amended) The flip-flop circuit of claim 1 ~~arrangement according to one of Claims 1 through 5~~, ~~characterized in that it~~ wherein the flip-flop circuit is implemented in emitter-coupled logic circuit technology.

7. (New) A shift register comprising the flip-flop circuit of claim 1.

8. (New) The flip-flop circuit of claim 2, wherein at least one of the first, the second, the third, and the fourth differential amplifiers and the first and the second switches are implemented using unipolar field effect circuit technology.

9. (New) A flip-flop circuit comprising

input terminals to provide a clock signal;

output terminals to provide an output signal,

a first differential amplifier comprising first emitter-coupled transistors having emitters connected to a first emitter node, the first emitter-coupled transistors comprising collector terminals that form at last parts of a first circuit node and a second circuit node, the first emitter-coupled transistors comprising base terminals that are cross-connected to collector terminals of the first emitter-coupled transistors;

a second differential amplifier comprising second emitter-coupled transistors having emitters connected to a second emitter node, the second emitter-coupled transistors comprising collector terminals that are connected to the first circuit node and/or to the second circuit node, the second emitter-coupled transistors comprising base terminals that form at least part of a third circuit node and a fourth circuit node;

a third differential amplifier comprising third emitter-coupled transistors having emitters connected to the second emitter node, the third emitter-coupled transistors comprising collector terminals that are connected to the third circuit node and/or to the fourth circuit node, the third emitter-coupled transistors comprising base terminals that are cross-connected to collector terminals of the third emitter-coupled transistors; and

a fourth differential amplifier comprising fourth emitter-coupled transistors having emitters connected to the first emitter node, the fourth emitter-coupled transistors comprising collector terminals that are connected to the third circuit node and/or to the fourth circuit node, the fourth emitter-coupled transistors comprising base terminals that are connected to the second circuit node and/or to the first circuit node;

a reference potential that is connectable to the first emitter node and to the second emitter node;

a first switch between a power supply potential terminal and the first emitter node, the first switch having a first control terminal that comprises part of the input terminals; and

a second switch between the supply potential terminal and the second emitter node, the second switch having a second control terminal that comprises part of the input terminals.

10. (New) The flip-flop circuit of claim 9, wherein the first, the second, the third, and the fourth circuit nodes are each connected via a resistor in a series circuit to the power supply potential terminal.

11. (New) The flip-flop circuit of claim 9, wherein the first, the second, the third, and the fourth differential amplifiers and the first and the second switches are implemented using bipolar circuit technology.

12. (New) The flip-flop circuit of claim 9, further comprising:

a first current source to connect the first emitter node to the reference potential terminal; and

a second current source to connect the second emitter node to the reference potential terminal.

13. (New) The flip-flop circuit of claim 12, wherein the first current source and the second current source each comprise a transistor implemented using metal oxide semiconductor circuit technology.

14. (New) The flip-flop circuit of claim 9, wherein the flip-flop circuit is implemented in emitter-coupled logic circuit technology.

15. (New) A shift register comprising the flip-flop circuit of claim 9.

16. (New) The flip-flop circuit of claim 9, wherein at least one of the first, the second, the third, and the fourth differential amplifiers and the first and the second switches are implemented using unipolar field effect circuit technology.